FEATURES

- **ST231 VLIW host CPU**
  - 333 MHz, 32 Kbyte ICache, 32 Kbyte DCache
  - up to 1.333 GOPs at 333 MHz
  - dynamic memory management through MMU
- **Unified memory interface**
- **Package 27 mm x 27 mm PBGA336**
  - footprint optimized for 2 layer PCBs
- **Dual transport stream merger**
  - supports DVB and DIRECTV®
  - integrated DES-ECB, DVB and ICAM descramblers
  - NDS RASP compliant
  - low-cost DVB-CI and Cable Card support
- **MPEG-2 MP@ML video decoder**
  - trick modes including smooth fast forward and rewind
- **Graphics/display**
  - 4 display planes
  - 2, 4 and 8 bpp CLUT graphics, 256 x 30 bits (AYCBCr) CLUT entries
  - 16 bpp true color graphics,
  - alpha blending, antialiasing, antiflutter, antiflicker filters
- **PAL/NTSC/SECAM encoder**
  - RGB, CVBS, Y/C and YUV outputs with 10-bit DACs
  - encoding of CGMS, Teletext, WSS, VPS, close caption
- **Audio subsystem**
  - MPEG-1 layers I/II, MP3
  - Dolby® Digital decoding
  - Dolby Pro Logic® compatible output
  - PCM input, mixing and sample rate conversion
  - SRS/TruSurroundXT® virtual surround sound
  - simultaneous MPEG audio decode and output of Dolby streams
- **On-chip peripherals**
  - 4 ASCs (UARTs) with Tx and Rx FIFOs
  - 6 parallel 8-bit I/O banks
  - 2 smartcard interfaces and clock generators
  - 3 SSCs for I^2C/SPI master/slave interfaces
  - SiLabs line side (DAA) interface
  - USB 1.1/2.0 host, OHCI/EHCI compliant
  - DiSEqC 2.0™ interface
- **Enhanced security**

PART NUMBERING

Table 1. Order codes

Part Number	Description
STi5300ZUA	Development version
STi5300AUA	Basic DVB
STi5300-Mboard	Development platform
STi5300-DVB	Software reference tree

REVISION HISTORY

Table 2. Revision history

Date	Revision	Description of changes
September-2005	1	First issue

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics.

All other names are the property of their respective owners

© 2005 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

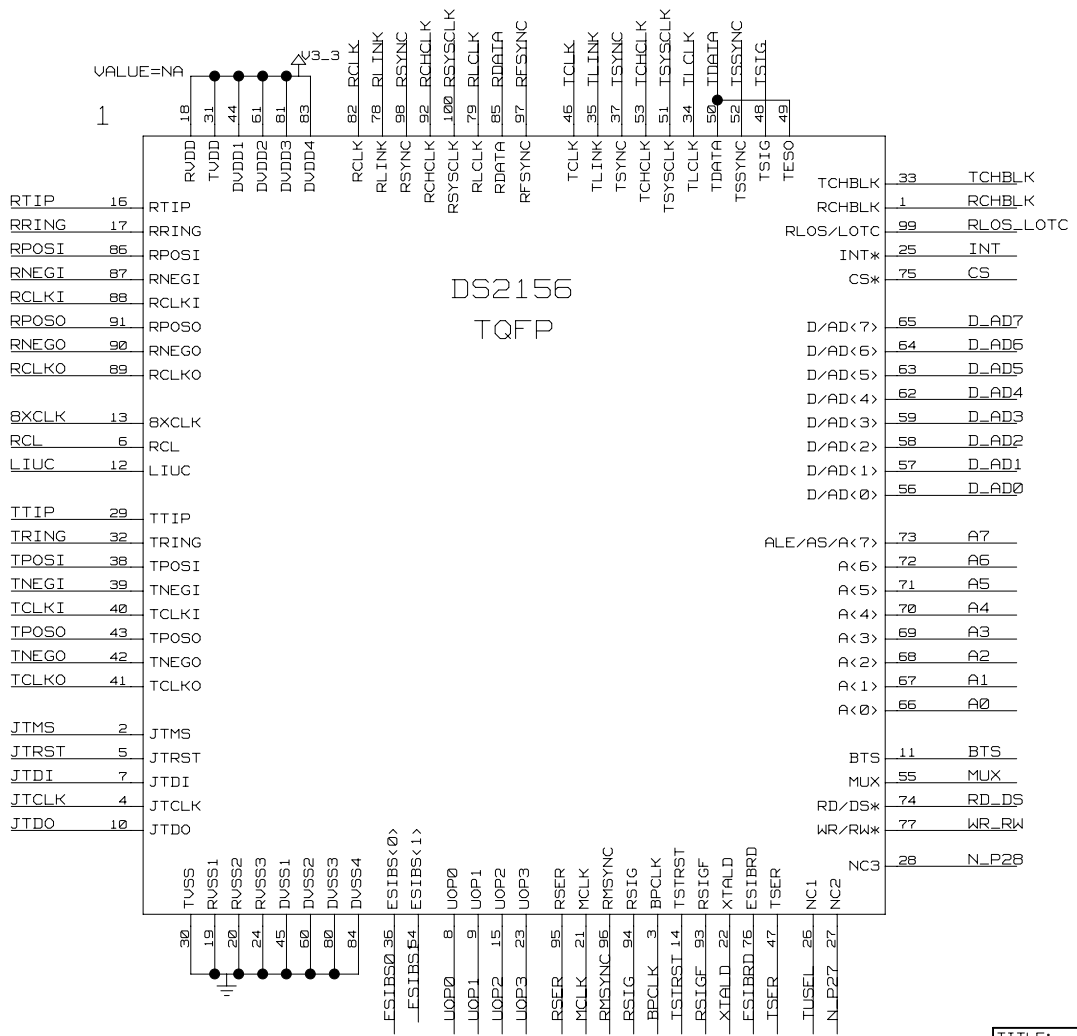
www.st.com

*** Signal Cross-Reference for the entire design ***

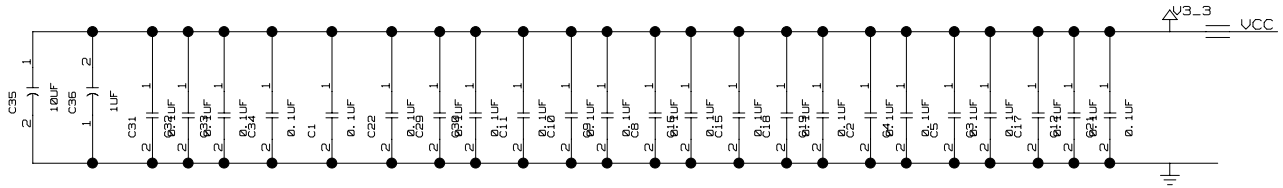
```
8XCLK              2C8> 11C7>
A0                 4C6<> 5C4<> 2B3< 11B3<
A1                 4C6<> 5C4<> 2B3< 11B3<
A2                 4C6<> 5C4<> 2B3< 11B3<
A3                 4C6<> 5C4<> 2B3< 11B3<
A4                 4C6<> 5C4<> 2B3< 11B3<
A5                 4C6<> 5C4<> 2B3< 11B3<
A6                 4C6<> 5C4<> 2B3< 11B3<
A7                 4C6<> 5C4<> 2B3< 11B3<
A8                 4C6<> 7B1<>
A9                 4B6<> 7B1<>
A10                4C3<> 7C3<>
A11                4C3<> 5C1<> 7C3<>
A12                4C3<> 5C1<> 7B3<>
A13                4B3<> 7B3<>
A14                4B3<>
A15                4B3<>
BPCLK              2A5> 8D4> 11A4>
BP_EN              5C1<> 6B2< 6B6< 6C2< 6C6<
BTS                5D4<> 2B3< 5A6< 11A3<
CLK1544_T          7B3<> 9D8<> 4B2<
CLK2048            5D3<> 9B3<> 9B6<>
CLK16384_T         4B4<> 5D3<> 7B3<>
CS                 5B4<> 2C3< 11C3<
CS_T               4B8<> 5B1<> 7B3<>
D_AD0              2B3<> 4B6<> 5C1<> 11B3<>
D_AD1              2C3<> 4B6<> 5C1<> 11B3<>
D_AD2              2C3<> 4B6<> 5C1<> 11C3<>
D_AD3              2C3<> 4B6<> 5C1<> 11C3<>
D_AD4              2C3<> 4B6<> 5C1<> 11C3<>
D_AD5              2C3<> 4B6<> 5C1<> 11C3<>
D_AD6              2C3<> 4A6<> 5C1<> 11C3<>
D_AD7              2C3<> 4A6<> 5D1<> 11C3<>
ESIBRD             2A5<> 11A4<> 5A8<
ESIBS0             2A6<> 11A6<>
ESIBS1             2A6<> 11A5<>
INT                2C3> 4A8<> 5A2<> 11C3> 5A6<
INT_INDICATOR      5A2<>
JTCLK              2A8< 11A7<
JTDI               2A8< 11A7<
JTDO               2A8> 11A7>
JTMS               2B8< 11B7<
JTRST              2B8< 5A8< 11A7<
LIUC               8B4> 2C8< 5A6< 11B7<
MCLK               9B6<> 9C6<> 2A5< 11A5<
MUX                5C4<> 2A3< 5A8< 11A3<
NIMD8              4B2<>
NIMD9              4B2<>
NIMD10             4B2<>
NIMD11             4B2<>
NIMD12             4B2<>
NIMD13             4B2<>
NIMD14             4B2<>
NIMD15             4C2<>
N_P27              2A4< 11A4<
N_P28              2A3< 11A3<
PPC_RSYNC          4C8<> 9A4<>
PPC_RXCLK          4C8<> 9A4<>
PPC_RXD            4C8<> 9A4<>
PPC_TDM_EN         5C1<> 9A4<
PPC_TSYNC          4B8<> 9A4<>
PPC_TXCLK          4C8<> 9A4<>
PPC_TXD            4C8<> 9A4<>
RCHBLK             2C3> 8D4> 11C3>
RCHCLK             2D6> 8D7> 11D5>
RCL                2C8> 11C7>
RCLK               2D6> 9A6<> 9C1<> 9C1<> 9D1<> 11D6>

RCLKI              8A7> 2C8< 5A8< 11C7<
RCLKO              2C8> 8A7> 11C7>
RDATA              2D6> 11D5>
RD_DS              5C4<> 2A3< 11A3<
RESET_OUT          4B6<> 5B1<> 7B1<>
RFSYNC             2D6> 8C7> 11D5>
RLCLK              2D6> 8B7> 11D5>

RLINK              2D6> 8B7> 11D6>
RLOS_LOTC          2C3> 5B2<> 11C3>
RLOS_LOTC_INDICATOR  5A2<>
RMSYNC             2A5> 8C7> 11A5>
RNEGI              8B7> 2C8< 5A8< 11C7<
RNEGO              2C8> 8A7> 11C7>
RPOSI              8B7> 2C8< 5A8< 11C7<
RPOSO              2C8> 8A7> 11C7>
RRING              2C8< 3B8< 11C7<
RSER               2A5> 8C7> 9A6<> 9B3<> 11A5>
RSIG               2A5> 8D7> 11A5>
RSIGF              2A5> 8D7> 11A4>
RSYNC              2D6<> 9A6<> 9B3<> 9C1<> 11D5<>
                  5A6<
RSYSCLK            9B6<> 9C3<> 9D6<> 2D6< 5A8< 11D5<
RTIP               2C8< 3B8< 11C7<
RW_T               4B6<> 5B1<> 7B1<>
RXADDR0            7B8<> 8D8
RXADDR1            7B6<> 8D8
RXADDR2            7B8<> 8D8
RXADDR3            7B8<> 8C8
RXADDR4            7B6<> 8C8
RXA_0              6B2<> 8D7>
RXA_1              6B7<> 8D7>
RXA_2_RXCLAV_1     6A7<> 6B2<> 8D7>
RXA_3_RXCLAV_2     6A7<> 6C7<> 8C7>
RXA_4_RXCLAV_3     6A7<> 6B2<> 8C7>
RXCLAV0            7A8<> 8C8
RXCLAV_0           6A7<> 8C7>
RXDATA_0           6B7<> 7C8<> 8B7> 8B8
RXDATA_1           6A2<> 7C6<> 8B7> 8B8
RXDATA_2           6B7<> 7C8<> 8B7> 8B8
RXDATA_3           6B2<> 7C6<> 8B7> 8B8
RXDATA_4           6B7<> 7C6<> 8A7> 8A8
RXDATA_5           6B2<> 7C8<> 8A7> 8A8
RXDATA_6           6B7<> 7C6<> 8A7> 8A8
RXDATA_7           6B2<> 7C8<> 8A7> 8A8
RXENA              6A2<> 8D4>
RXENB              7A6<> 8D5
RXPRTY             6B5<>
RXSOC              6B7<> 7B6<> 8D4> 8D5
SNIM_B2            4C2<>
SNIM_B3            4C2<>
SNIM_B4            4C2<>
SNIM_B5            4C2<>
SNIM_B6            4C2<>
SNIM_B7            4C2<>
SW1_B0EN           5A4<> 9D8<
SW1_B1EN           5A4<> 9D8<
SW1_B2EN           5A3<> 9D6<
SW1_B3EN           5A3<> 9D6<
SW2_B0EN           5A3<> 9B8<
SW2_B1EN           5A3<> 9B8<
SW2_B2EN           5A3<> 9B6<
SW2_B3EN           5A3<> 9B6<
SW3_B0EN           5A3<> 9D3<
SW3_B1EN           5A3<> 9D3<
SW3_B2EN           5A3<> 9D1<
SW3_B3EN           5A3<> 9D1<
SW4_B0EN           5B4<> 9B3<
SW4_B1EN           5B4<> 9B3<
SW4_B2EN           5B4<> 9B2<
SW4_B3EN           5B4<> 9B2<
TCHBLK             2D3> 8C4> 11C3>
TCHCLK             2D5> 11D4> 8A1<
TCK                5B8<> 5D8<
TCLK               9A6<> 9B6<> 9C3<> 9C6<> 2D5< 5A6<
                  11D5<
TCLKI              8B4> 2B8< 5A8< 11B7<
TCLKO              2B8> 8A4> 11B7>
TDATA              2D5<> 11D4<>
TDI                5B8<> 5D7<
TDO                5B8<> 5C7<
TIMSV              4D3<> 4D8<>
TLCLK              2D5> 8C4> 11D4>
TLINK              8C4> 2D5< 5B6< 11D5<
TMS                5B8<> 5C7<

TNEGI              8B4> 2B8< 5A8< 11B7<
TNEGO              2B8> 8A4> 11B7>
TPOSI              8C4> 2B8< 5A8< 11B7<
TPOSO              2B8> 8A4> 11B7>
TRING              2B8> 11B7> 3C8<
TSER               8A4> 9A6<> 9B2<> 2A5< 5A8< 11A4<
TSIG               8D1> 2D5< 5B6< 11D4<
TSSYNC             9C3<> 2D5< 5B6< 8A1< 11D4<
TSTRST             2A5< 5A8< 11A4<
TSYNC              2D5<> 9A6<> 9B2<> 11D5<> 5A6<
TSYSCLK            8D1> 9B6<> 9D3<> 9D6<> 2D5< 5A8<
                  11D4<
TTIP               2B8> 11B7> 3C8<
TUSEL              5D2<> 2A4< 11A4<
TXADDR0            7B5<> 8D5
TXADDR1            7B4<> 8C5
TXADDR2            7B4<> 8C5
TXADDR3            7B5<> 8C5
TXADDR4            7B4<> 8C5
TXA_0              6C2<> 8D4>
TXA_1              6C7<> 8C4>
TXA_2_TXCLAV_1     6B2<> 6C2<> 8C4>
TXA_3_TXCLAV_2     6C7<> 6C7<> 8C4>
TXA_4_TXCLAV_3     6C2<> 6C2<> 8C4>
TXCLAV0            7B5<> 8B5
TXCLAV_0           6C7<> 8B5
TXDATA_0           6C7<> 7C5<> 8B4> 8B5
TXDATA_1           6C2<> 7C4<> 8B4> 8B5
TXDATA_2           6C7<> 7C5<> 8A4> 8A5
TXDATA_3           6C2<> 7C4<> 8A4> 8A5
TXDATA_4           6C7<> 7C4<> 8A4> 8A5
TXDATA_5           6C2<> 7C5<> 8A4> 8A5
TXDATA_6           6C7<> 7C4<> 8D1> 8D2
TXDATA_7           6C2<> 7C5<> 8D1> 8D2
TXENA              6C2<> 8C1>
TXENABLE           7B4<> 8C2
TXPRTY             6C5<>
TXSOC              6C7<> 7B4<> 8B1> 8B2
UOP0               2A6> 8B1> 11A5>
UOP1               2A6> 8C1> 11A5>
UOP2               2A6> 11A5>
UOP3               2A6> 8D4> 11A5>
UR_ADDR0           8D8
UR_ADDR1           8D8
UR_ADDR2           8D8
UR_ADDR3           8C8
UR_ADDR4           8C8
UR_CLAV            8C8
UR_CLK             9B2<> 6A1< 7A8< 8A2<
UR_DATA0           8B8
UR_DATA1           8B8
UR_DATA2           8B8
UR_DATA3           8B8
UR_DATA4           8A8
UR_DATA5           8A8
UR_DATA6           8A8
UR_DATA7           8A8
UR_ENB             8D5
UR_SOC             8D5
UT_ADDR0           8D5
UT_ADDR1           8C5
UT_ADDR2           8C5
UT_ADDR3           8C5
UT_ADDR4           8C5
UT_CLAV            8B4>
UT_CLK             9B2<> 6C1< 7B4< 8A2<
UT_DATA0           8B5
UT_DATA1           8B5
UT_DATA2           8A5
UT_DATA3           8A5
UT_DATA4           8A5
UT_DATA5           8A5
UT_DATA6           8D2
UT_DATA7           8D2
UT_ENB             8C2
UT_SOC             8B2
WE_T               4B6<> 5B1<> 7B1<>
```

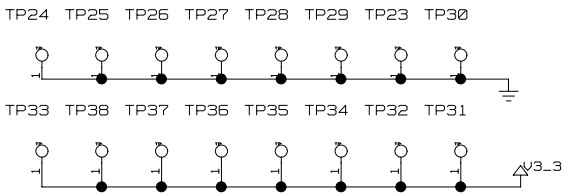
```
WR_RW              5C4<> 2A3< 11A3<
XTALD              2A5> 11A4>
```

TITLE: DS2156DK02A0	DATE: 10/04/02
ENGINEER: SWS	PAGE: 12/13

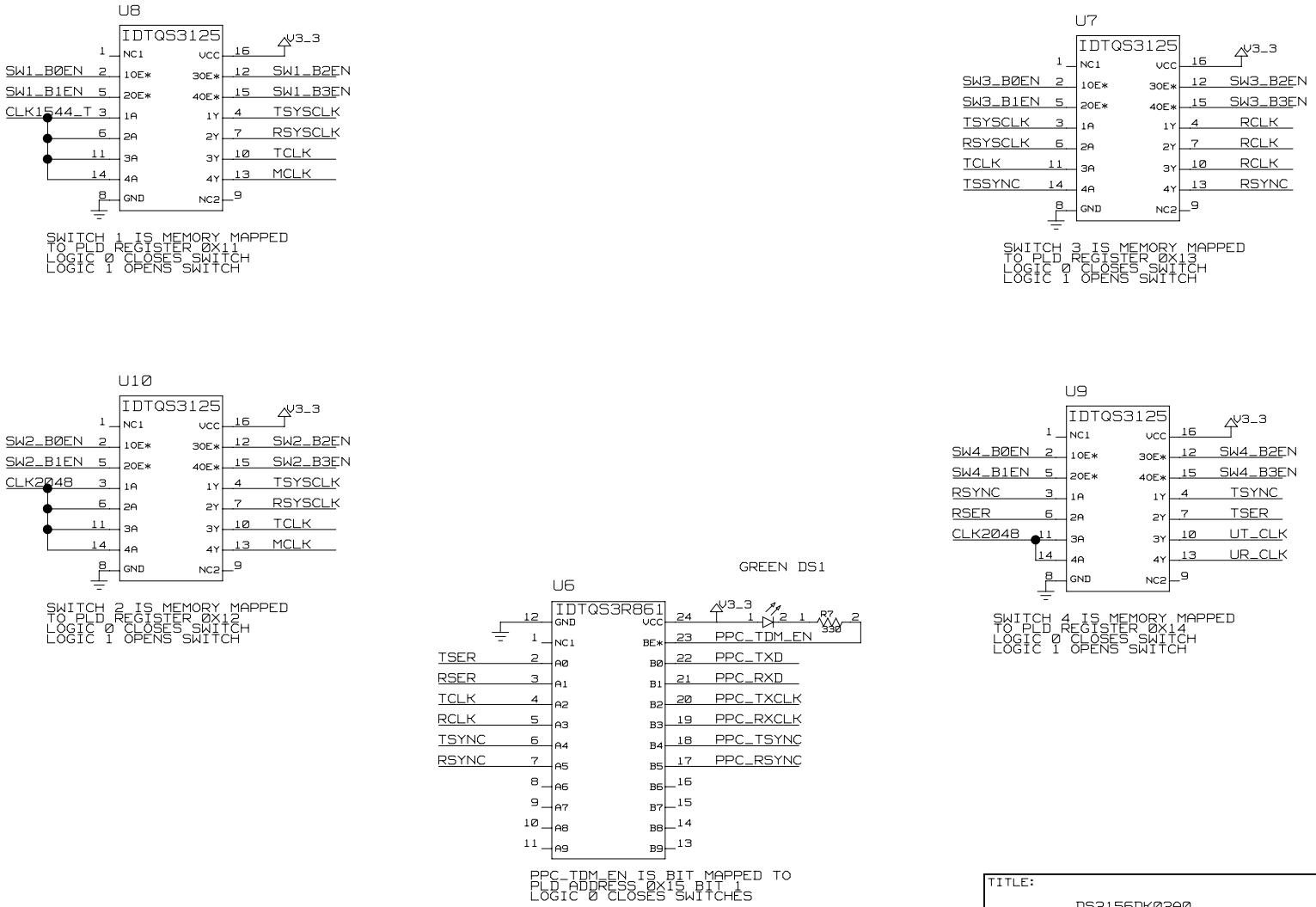


TITLE: DS2156DK02A0	DATE: 10/04/02
ENGINEER: SWS	PAGE: 11/13





TITLE: DS2156DK02A0	DATE: 10/04/02
ENGINEER: SWS	PAGE: 10/13



TITLE: DS2156DK02A0	DATE: 10/04/02
ENGINEER: SWS	PAGE: 9 /13

RXADDR0 — RXA_0
UR_ADDR0 — RCHCLK

RXADDR1 — RXA_1
UR_ADDR1 — RSIGF

RXADDR2 — RXA_2_RXCLAV_1
UR_ADDR2 — RSIG

RXADDR3 — RXA_3_RXCLAV_2
UR_ADDR3 — RMSYNC

RXADDR4 — RXA_4_RXCLAV_3
UR_ADDR4 — RFSYNC

RXCLAV0 — RXCLAV_0
UR_CLAV — RSER

RXDATA_0 — RXDATA_0
UR_DATA0 — RLINK

RXDATA_1 — RXDATA_1
UR_DATA1 — RLCLK

RXDATA_2 — RXDATA_2
UR_DATA2 — RPOSI

RXDATA_3 — RXDATA_3
UR_DATA3 — RNEGI

RXDATA_4 — RXDATA_4
UR_DATA4 — RCLKI

RXDATA_5 — RXDATA_5
UR_DATA5 — RCLKO

RXDATA_6 — RXDATA_6
UR_DATA6 — RNEGO

RXDATA_7 — RXDATA_7
UR_DATA7 — RPOSO

RXENB — RXENA
UR_ENB — BPCLK

RXSOC — RXSOC
UR_SOC — RCHBLK

TXADDR0 — TXA_0
UT_ADDR0 — UOP3

TXADDR1 — TXA_1
UT_ADDR1 — TCHBLK

TXADDR2 — TXA_2_TXCLAV_1
UT_ADDR2 — TLCLK

TXADDR3 — TXA_3_TXCLAV_2
UT_ADDR3 — TLINK

TXADDR4 — TXA_4_TXCLAV_3
UT_ADDR4 — TPOSI

TXCLAV0 — UT_CLAV
TXCLAV_0 — LIUC

TXDATA_0 — TXDATA_0
UT_DATA0 — TNEGI

TXDATA_1 — TXDATA_1
UT_DATA1 — TCLKI

TXDATA_2 — TXDATA_2
UT_DATA2 — TCLKO

TXDATA_3 — TXDATA_3
UT_DATA3 — TNEGO

TXDATA_4 — TXDATA_4
UT_DATA4 — TPOSO

TXDATA_5 — TXDATA_5
UT_DATA5 — TSER

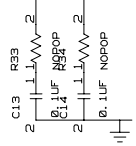
TXDATA_6 — TXDATA_6
UT_DATA6 — TSIG

TXDATA_7 — TXDATA_7
UT_DATA7 — TSYSCLK

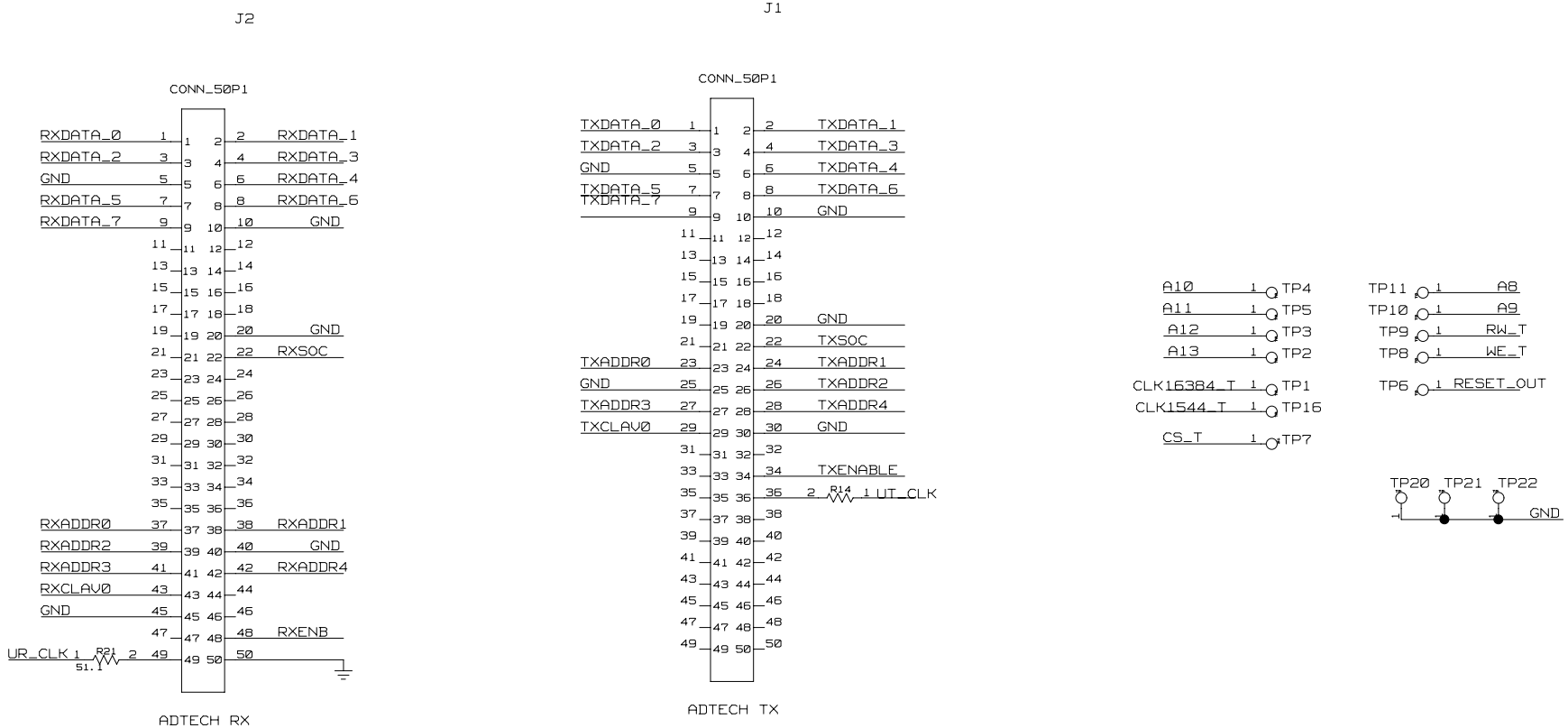
TXENABLE — TXENA
UT_ENB — UOP1

TXSOC — TXSOC
UT_SOC — UOP0

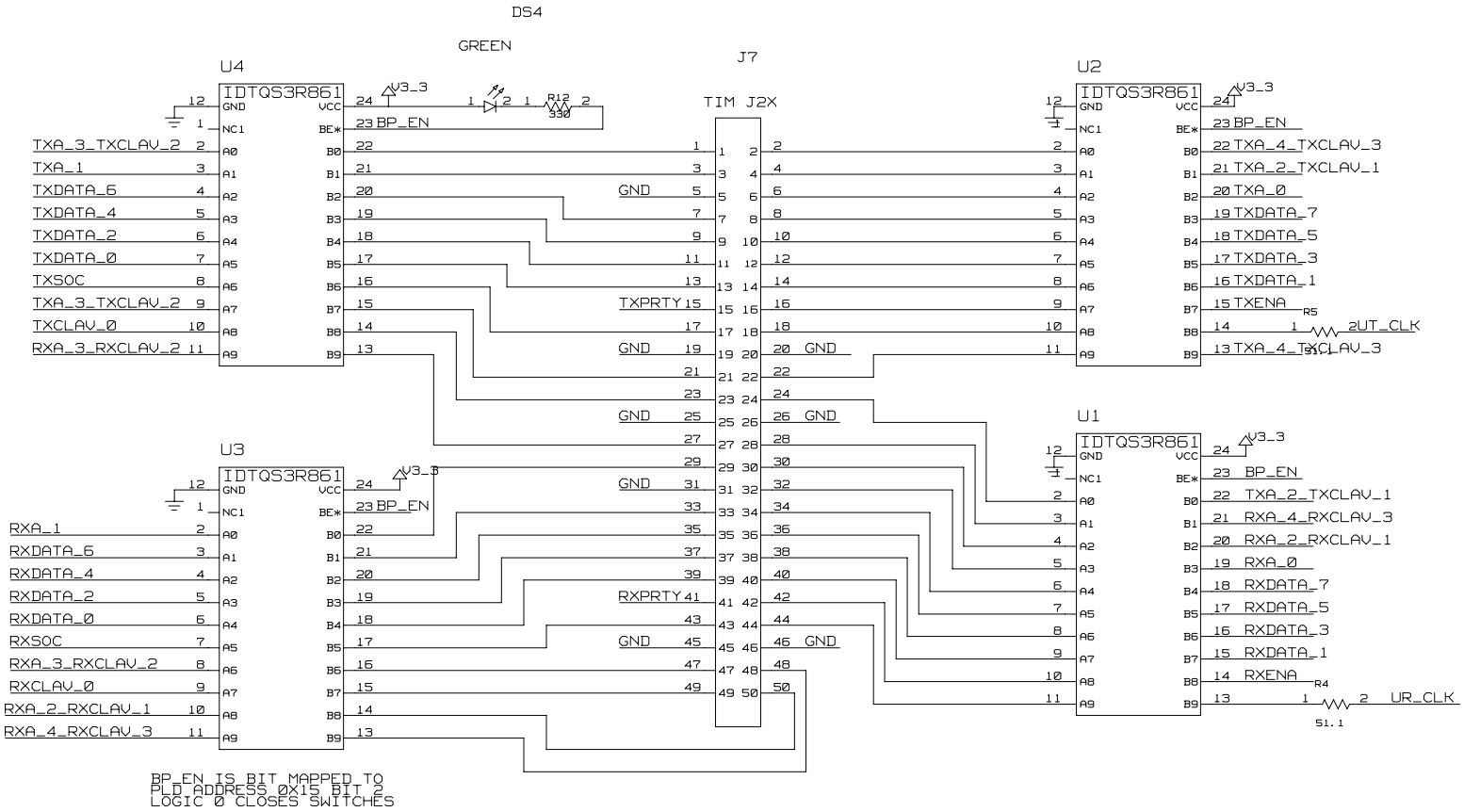
UT_CLK — TSSYNC
UR_CLK — TCHCLK



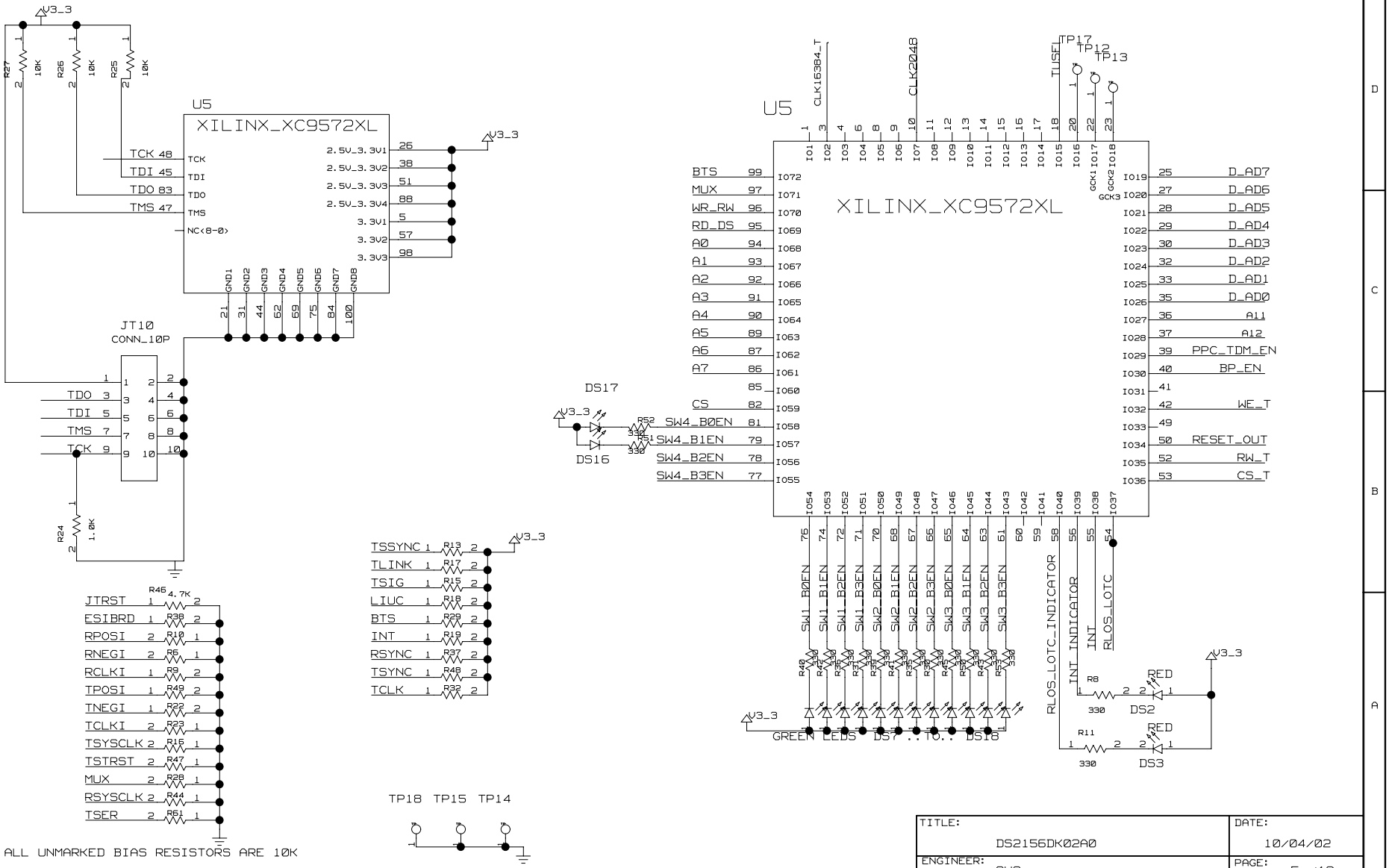
TITLE: DS2156DK02A0	DATE: 10/04/02
ENGINEER: SWS	PAGE: 8 /13

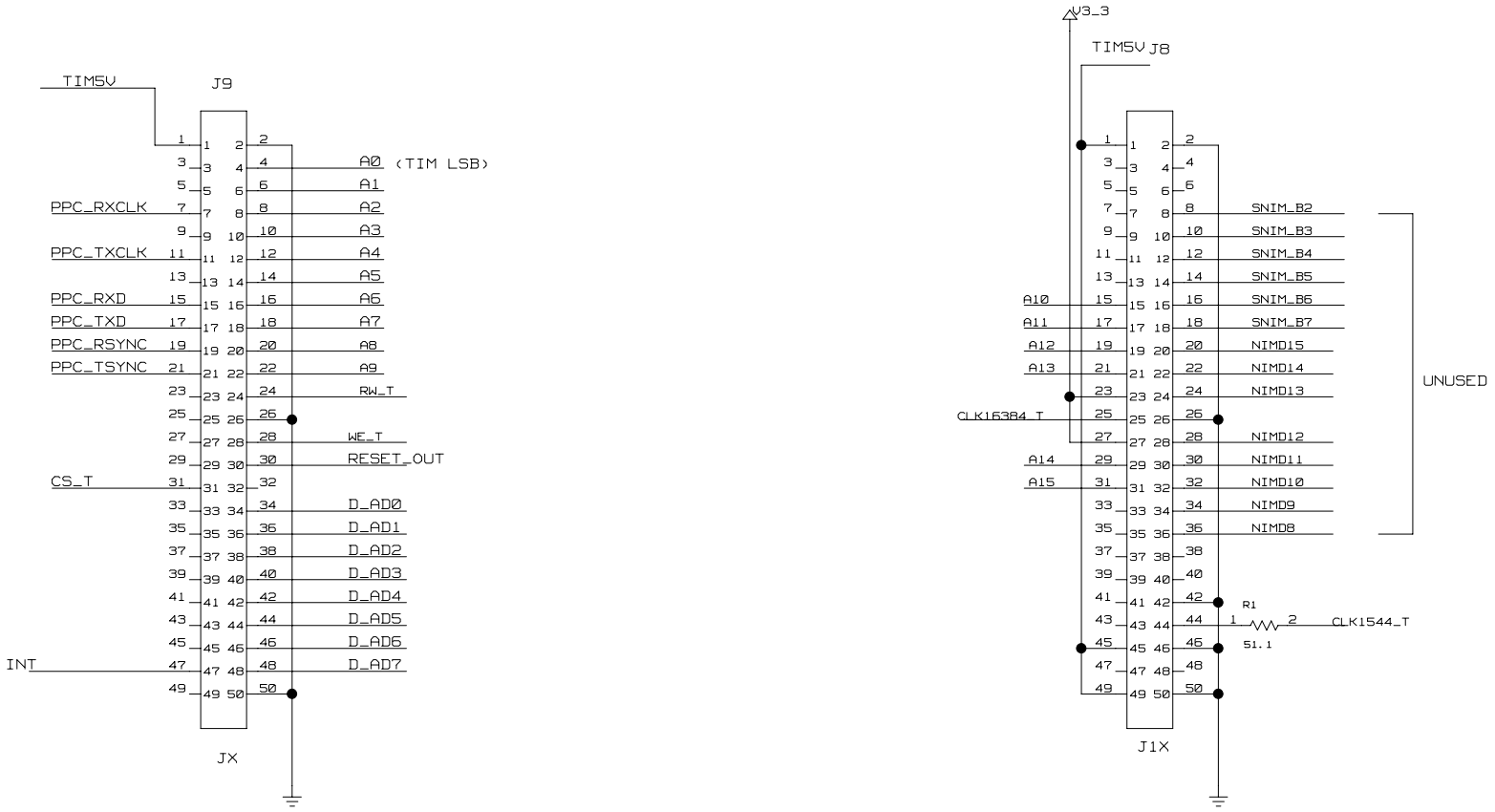


TITLE: DS2156DK02A0	DATE: 10/04/02
ENGINEER: SWS	PAGE: 7 /13

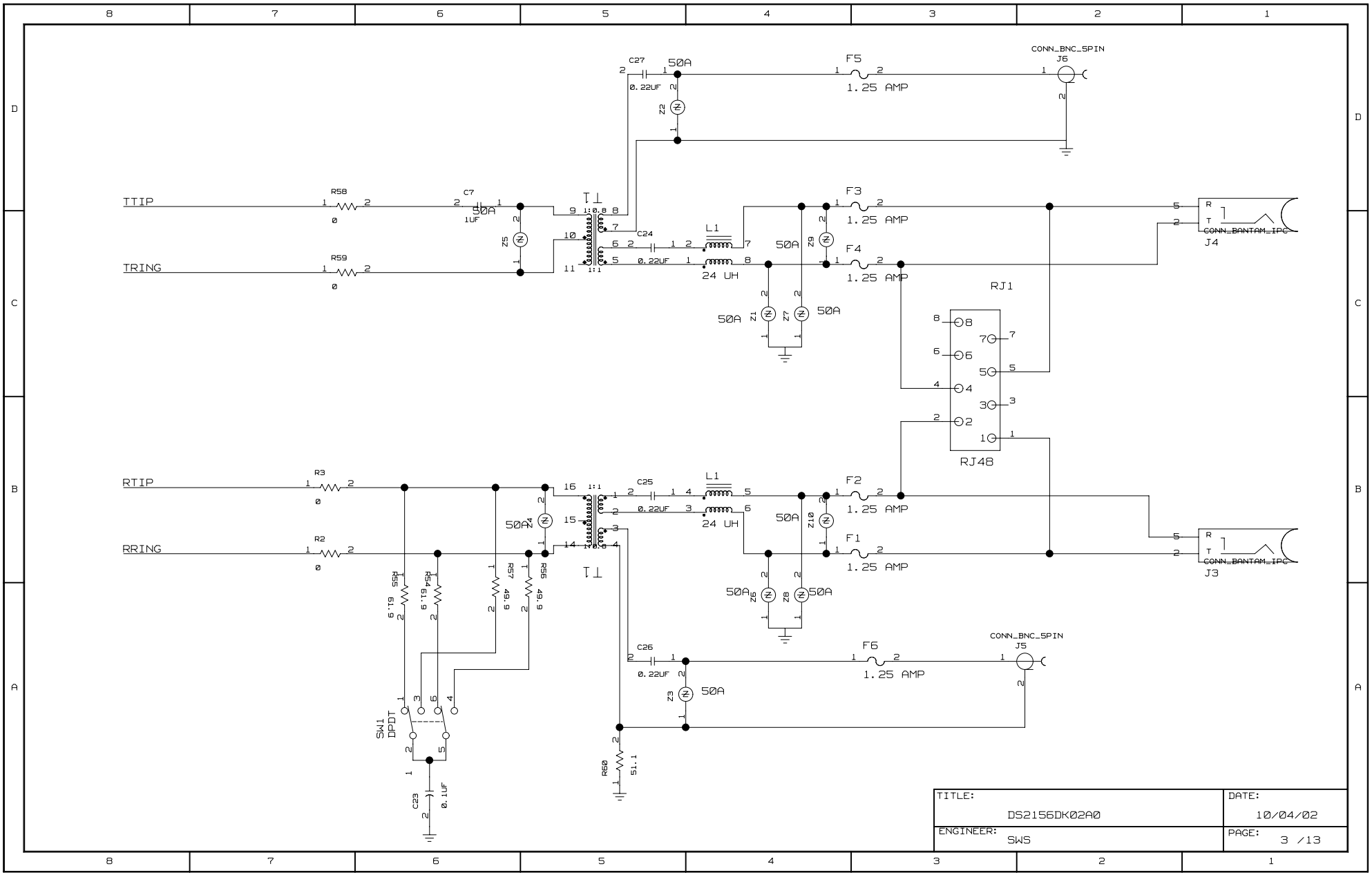


TITLE: DS2156DK02A0	DATE: 10/04/02
ENGINEER: SWS	PAGE: 6 /13

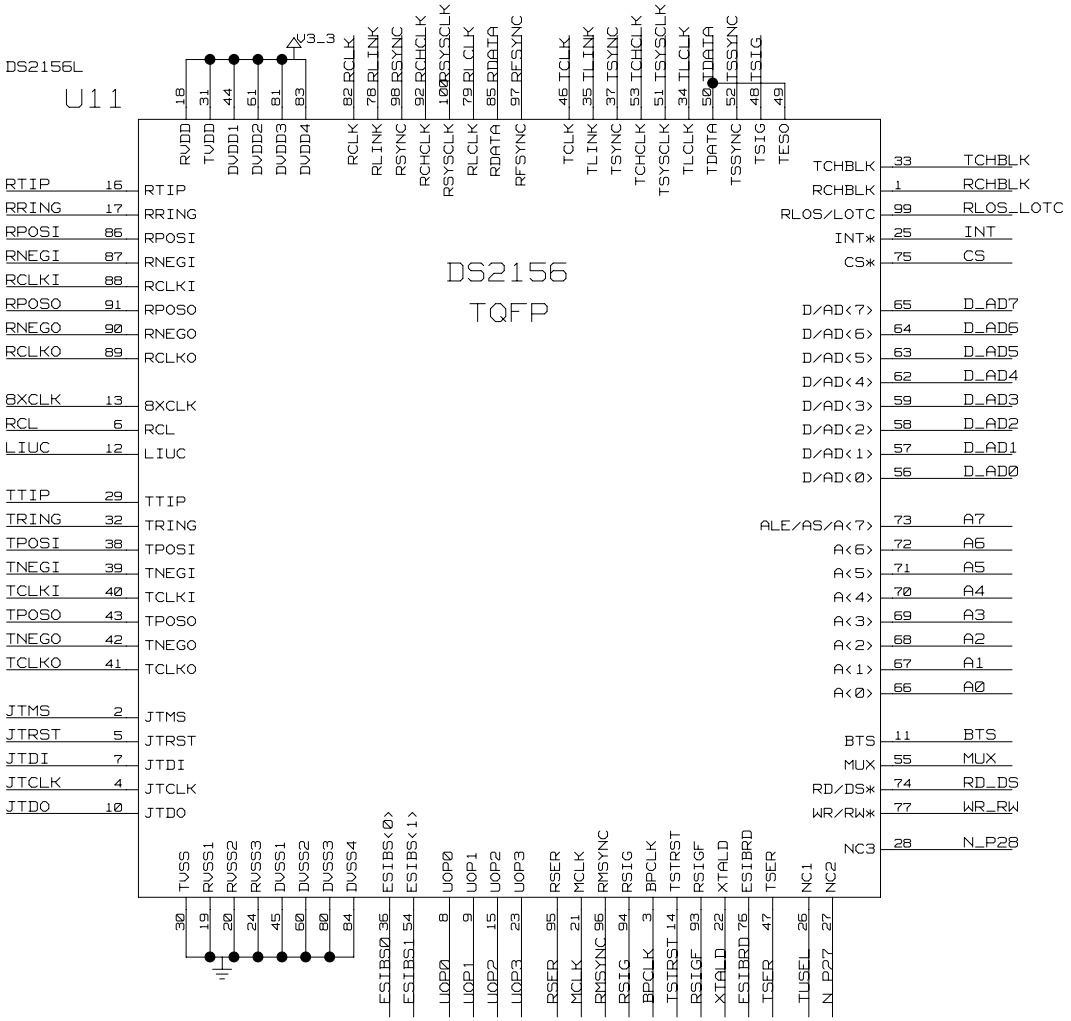

U5
XILINX_XC9572XL
JT10
CONN_10P
DS17
DS16
GREEN LEDS DS7 .. TO.. DS18
DS2
DS3
RED
ALL UNMARKED BIAS RESISTORS ARE 10K
TP18 TP15 TP14
TP17
TP12
TP13
TITLE:
DS2156DK02A0
DATE:
10/04/02
ENGINEER:
SWS
PAGE:
5 /13



TITLE: DS2156DK02A0	DATE: 10/04/02
ENGINEER: SWS	PAGE: 4 /13



TITLE: DS2156DK02A0	DATE: 10/04/02
ENGINEER: SWS	PAGE: 3 /13



TITLE: DS2156DK02A0	DATE: 10/04/02
ENGINEER: SWS	PAGE: 2 /13

DS2156, DS2155, DS2135Y DESIGN KIT

CONTENTS

1. COVER PAGE
2. SCT POPULATION OPTION (DS2155, DS2156, DS21352 OR DS21354)
3. TX AND RX ANALOG PATHS
4. TIM ADDRESS AND DATA BUS
5. CPLD ADDRESS DATA CONNECTIONS, BIAS LEVELS FOR SCT
6. UTOPIA: TIM HEADER AND BUS SWITCHES
7. TESTPOINTS FOR UTOPIA 2
8. UTOPIA: NETLIST ASSOCIATIONS
9. SWITCHING FOR CLOCKS AND TDM
10. SUPPLY DECOUPLING
11. SCT TESTPOINTS
12. NETLIST CROSS-REFERENCE
13. PART CROSS-REFERENCE

TITLE: DS2156DK02A0	DATE: 10/04/02
ENGINEER: SWS	PAGE: 1 /13